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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/073,494	05/06/1998	PAI-HUNG PAN	2915.1US(96-	9834

7590 11/03/2003  
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EXAMINER

VU, HUNG K

ART UNIT	PAPER NUMBER
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2811

DATE MAILED: 11/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/073,494

Applicant(s)

PAN ET AL.

Examiner

Hung K. Vu

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*file*

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(e). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 16 July 2003.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 23-33 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 23-33 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413) Paper No(s) \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### *Request for Continued Examination*

1 A request for continued examination (RCE) under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicants' submission filed on 07/16/03 has been entered. An action on the RCE follows.

### *Claim Rejections - 35 USC § 103*

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 23-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. (PN 5,472,896, of record) in view of Tomozawa et al. (PN 4,782,037).

With regard to claim 23, Chen et al. discloses an operable gate stack on a silicon substrate having a dielectric layer thereover, the dielectric layer being substantially devoid of pitting, the operable gate stack including a non-crystalline metallic silicide film (16) and a dielectric cap (22) on the non-crystalline metallic silicide film. Note Col. 4, lines 23-50 and Figures 1e and 3f. Also note

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that because a metallic silicide film (16) is in an amorphous state, it is inherent that the dielectric layer is substantially devoid of pitting.

Chen et al. discloses the dielectric cap is formed of oxide. Chen et al. does not disclose the dielectric cap is formed of silicon nitride. However, Tomozawa et al. discloses a dielectric cap (11) is formed of oxide or silicon nitride. Note Figures 1B and 9, and Col. 4, lines 45-54.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to substitute the oxide of Chen et al. by the silicon nitride of Tomozawa et al. because oxide and silicon nitride are commonly used as the material for the dielectric cap and they are interchangeable.

With regard to claim 24, Chen et al. discloses an operable gate stack on a silicon substrate having a dielectric layer thereover, the dielectric layer being substantially devoid of pitting, the operable gate stack, including an amorphous metallic silicide film (16) wherein the metallic silicide film is substantially devoid of silicon clusters, a dielectric cap (22) on the non-crystalline metallic silicide film. Note Col. 4, lines 23-50 and Figures 1e and 3f. Also note that because the metallic silicide film is in an amorphous state, it is inherent that it is substantially devoid of silicon clusters and the dielectric layer is substantially devoid of pitting.

Chen et al. discloses the dielectric cap is formed of oxide. Chen et al. does not disclose the dielectric cap is formed of silicon nitride. However, Tomozawa et al. discloses a dielectric cap (11) is formed of oxide or silicon nitride. Note Figures 1B and 9, and Col. 4, lines 45-54.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to substitute the oxide of Chen et al. by the silicon nitride of Tomozawa et al. because

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oxide and silicon nitride are commonly used as the material for the dielectric cap and they are interchangeable.

With regard to claim 25, Chen et al. discloses an operable gate stack on a silicon substrate (10) having a dielectric layer (12) thereover, the dielectric layer being substantially devoid of pitting, the operable gate stack comprising,

a polysilicon layer (14) disposed over the dielectric layer;

a non-crystalline metallic silicide film (16) disposed over the polysilicon layer;

a dielectric cap (22) on the non-crystalline metallic silicide film. Note Col. 4, lines 23-50 and Figures 1e and 3f. Also note that because the metallic silicide film is in an amorphous state, it is inherent that it is substantially devoid of silicon clusters and the dielectric layer is substantially devoid of pitting.

Chen et al. discloses the dielectric cap is formed of oxide. Chen et al. does not disclose the dielectric cap is formed of silicon nitride. However, Tomozawa et al. discloses a dielectric cap (11) is formed of oxide or silicon nitride. Note Figures 1B and 9, and Col. 4, lines 45-54.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to substitute the oxide of Chen et al. by the silicon nitride of Tomozawa et al. because oxide and silicon nitride are commonly used as the material for the dielectric cap and they are interchangeable.

With regard to claim 26, Chen et al. discloses a gate stack structure comprising an operable gate stack on a dielectric layer (12), over a silicon substrate (10), wherein the dielectric layer is

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substantially devoid of pitting, the operable gate stack comprising a metallic silicide film (16) and a dielectric cap (22) on the metallic silicide film. Note that because a metallic silicide film (16) is in an amorphous state, it is inherent that the dielectric layer is substantially devoid of pitting. Note Col. 4, lines 23-50 and Figures 1e and 3f.

Chen et al. discloses the dielectric cap is formed of oxide. Chen et al. does not disclose the dielectric cap is formed of silicon nitride. However, Tomozawa et al. discloses a dielectric cap (11) is formed of oxide or silicon nitride. Note Figures 1B and 9, and Col. 4, lines 45-54.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to substitute the oxide of Chen et al. by the silicon nitride of Tomozawa et al. because oxide and silicon nitride are commonly used as the material for the dielectric cap and they are interchangeable.

With regard to claim 27, Chen et al. and Tomozawa et al. disclose the metallic silicide film comprises a non-crystalline metallic silicide film (16).

With regard to claim 28, Chen et al. and Tomozawa et al. disclose the metallic silicide film comprises an amorphous metallic silicide film (16) substantially devoid of silicon clusters. Note that because the metallic silicide film is in an amorphous state, it is inherent that it is substantially devoid of silicon clusters.

With regard to claim 29, Chen et al. discloses a semiconductor device comprising at least one gate stack formed on a silicon substrate having a dielectric layer thereover, the dielectric layer

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being substantially devoid of pitting, the at least one gate stack comprising a non-crystalline metallic silicide film (16) and a dielectric cap (22) on the non-crystalline metallic silicide film. Note Col. 4, lines 23-50 and Figures 1e and 3f. Also note that because a metallic silicide film (16) is in an amorphous state, it is inherent that the dielectric layer is substantially devoid of pitting.

Chen et al. discloses the dielectric cap is formed of oxide. Chen et al. does not disclose the dielectric cap is formed of silicon nitride. However, Tomozawa et al. discloses a dielectric cap (11) is formed of oxide or silicon nitride. Note Figures 1B and 9, and Col. 4, lines 45-54.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to substitute the oxide of Chen et al. by the silicon nitride of Tomozawa et al. because oxide and silicon nitride are commonly used as the material for the dielectric cap and they are interchangeable.

With regard to claim 30, Chen et al. and Tomozawa et al. disclose the at least one gate stack further comprising,

a polysilicon layer (14) disposed over the dielectric layer,

the non-crystalline metallic silicide film (16) being disposed over the polysilicon layer.

With regard to claim 31, Chen et al. discloses a semiconductor device comprising at least one gate stack structure on a dielectric layer (12), over a silicon substrate (10), wherein the dielectric layer is substantially devoid of pitting, the at least one gate stack structure comprising a metallic silicide film (16) and a dielectric cap (22) on the metallic silicide film. Note Col. 4, lines 23-50

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and Figures 1e and 3f. Also note that because a metallic silicide film (16) is in an amorphous state, it is inherent that the dielectric layer is substantially devoid of pitting.

Chen et al. discloses the dielectric cap is formed of oxide. Chen et al. does not disclose the dielectric cap is formed of silicon nitride. However, Tomozawa et al. discloses a dielectric cap (11) is formed of oxide or silicon nitride. Note Figures 1B and 9, and Col. 4, lines 45-54.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to substitute the oxide of Chen et al. by the silicon nitride of Tomozawa et al. because oxide and silicon nitride are commonly used as the material for the dielectric cap and they are interchangeable.

With regard to claim 32, Chen et al. and Tomozawa et al. disclose the metallic silicide film comprises a non-crystalline metallic silicide film (16).

With regard to claim 33, Chen et al. and Tomozawa et al. disclose the metallic silicide film comprises an amorphous metallic silicide film (16) substantially devoid of silicon clusters. Note that because the metallic silicide film is in an amorphous state, it is inherent that it is substantially devoid of silicon clusters.

### ***Response to Arguments***

3. Applicant's arguments with respect to claims 23-33 have been considered but are moot in view of the new ground(s) of rejection.



***Conclusion***

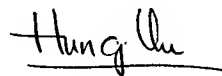
4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hung K. Vu whose telephone number is (703) 308-4079. The examiner can normally be reached on Mon-Thurs 6:00-3:30, alternate Friday 7:00-3:30, Eastern Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (703) 308-1690. The Central Fax Number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Vu

October 30, 2003



Hung Vu

Patent Examiner